Marked up paragraph at page 10, lines 3-14.

Referring now to the drawings, and more particularly to Figure 1, there is shown a high-level block diagram of an exemplary architecture of a programmable memory BIST module. (It should understood that the depiction of Figures 1-3 are arranged to convey an understanding of the invention and are not admitted to be prior art as to the present invention.) Central to this architecture is a programmable memory BIST controller 10 which preferably includes a microcode based controller 100, an instruction sore module 30 (both shown in Figure 3 and an instruction decode module 20).

Marked up paragraph at page 12, lines 17-29.

If, on the other hand, the test is of the board level type, a bit string in accordance with the IEEE 1149.1 standard is created, as indicated at 145, and an appropriate IEEE 1149.1 instruction is loaded into the instruction store module as instructions by applying an appropriate number of clock cycles, as indicated at 150. The bi t string is then applied to the test data interface (TDI), as indicated at 155 and the test access port (TAP) controller is set to the SHIFT-DR state, as indicated at 160 and an appropriate number of clock cycles are applied to transfer the bit string into the instruction store module 30 as indicated at [160] 165.

IN THE CLAIMS:

Please amend claims 1, 8, and 12 as follows. A clean copy of amended claims1, 8, and 12 is provided in the attached separate sheet, entitled "Clean Copy of Amended Claims."

Claim 1 (Amended). An integrated circuit including an embedded memory and a built-in self-test arrangement including

means for storing test instructions including means for discriminating a source of a test command and receiving test instructions provided from an external tester,

means for generating default test instructions, and